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EXAMINER	
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ART UNIT	**PAPER NUMBER**
2655	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/996,929	YAMAZAKI ET AL.
	Examiner	Art Unit
	Brian L. Albertalli	2655

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: --Apparatus Including an Error Detector and a Limiter for Decoding an Adaptive Differential Pulse Code Modulation Receiving Signal--.

Claim Objections

2. Claims 11 and claim 13 are objected to because of the following informalities:

In line 8 of claim 11, "outputs" should be –output--.

In line 7 of claim 13, "outputs" should be –output--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 4-6 and 13-18 are replete with antecedent basis errors and inconsistencies and thus are rejected under 35 USC 112, second paragraph.

For example, claim 4 includes the limitation "a third comparator" and "third comparison result", but a first and second comparator and first and second comparison result are not established in the parent claim (claim 1). While claims 2 and 3 include a first comparator and second comparator, claim 4 does not depend from these claims,

therefore a "third" comparator is inconsistent with the parent claim. Similarly, claim 5 includes the limitation "a third logic circuit" when first and second logic circuits are not established in either claims 1 or 4 (from which claim 5 depends).

Similarly, independent claim 16 includes the limitation "a second threshold value setting portion", when there is no other mention of a "threshold value setting portion" in the claim.

Claims 6, 13-15, and 17-18 are replete with similar errors (e.g. "a fourth output" claimed when no first, second, or third output has been established), and these inconsistencies must be corrected.

For the purposes of examination, the Examiner has interpreted the claims so as to primarily ignore the numerical designation to each claimed component (first output, second output, etc.) and matched the claimed components to the prior art as best as possible.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Walley et al. (U.S. Patent 5,896,576).

In regard to claim 1, Walley et al. disclose an apparatus for decoding encoded voice data (Fig. 1) comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (modem 13, column 2, lines 21-30);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (ADPCM decoder 15, column 2, lines 31-34);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (modem 13 provides an error flag indicator, column 2, lines 27-30); and

a limiter which outputs either said pulse code modulation data or a limit data in accordance with said detection result (clipping circuit 25 activates when an error is detected, column 2, lines 47-52 and lines 56-63).

7. Claims 1-7 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Murata et al. (U.S. Patent 5,925,146).

In regard to claim 1, Murata et al. disclose an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (1c, column 1, lines 35-38);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25); and

a limiter (clipper) which outputs either said pulse code modulation data or a limit data in accordance with said detection result (Fig. 24, clip processor 11 limits the amplitude of the PCM code to the clip value signal 114, column 24, lines 49-65).

In regard to claim 2, Murata et al. disclose said limit data has an upper limit data (Fig. 25, upper clip value 114) and a lower limit data (lower clip value 114); and wherein said limiter comprises:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result (Fig. 26, comparator 11a compares the positive amplitude of input PCM data with the clip value 114, column 26, lines 7-19);

a second comparator which compares said pulse code modulation data and said lower limit data and which outputs a second comparison result (comparator 11a compares the negative amplitude of the PCM data with the clip value 114, column 26, lines 7-19); and

a first output portion which outputs said pulse code modulation data, said upper limit data or said lower limit data in accordance with said detection result and said first and second comparison results (when the PCM amplitude is greater than the clip value, the clip value is output with the appropriate sign, i.e. positive or negative; when the PCM amplitude is less than the clip value, the PCM data is output, column 26, lines 7-19).

In regard to claim 3, Murata et al. disclose said first output portion comprises:

a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second logic circuit which outputs a second logic circuit result having said first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level (similarly, the negative comparison results are only activated in response to the error detection information 102, and thus the circuits are equivalent, column 25, lines 46-62); and

a first selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, said lower limit data when said second logic

circuit result having said first voltage level is input or said pulse code modulation data when said first and second logic circuit results each not having said first voltage level is input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62).

In regard to claim 4, Murata et al. discloses a format of said limit data is the absolute value (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, therefore, the clip value must be an absolute value, column 26, lines 17-19); and wherein said limiter portion comprises:

a third comparator which compares a numerical value data of said pulse code modulation data and said limit data and which outputs a third comparison result (Fig. 26, comparator 11a, column 26, lines 7-19); and

a second output portion which outputs said pulse code modulation data or said limit data in accordance with said detection result and said third comparison result (when the PCM amplitude is greater than the clip value, the clip value is output with the appropriate sign, i.e. positive or negative; when the PCM amplitude is less than the clip value, the PCM data is output, column 26, lines 7-19).

In regard to claim 5, Murata et al. discloses said second output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said

detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second selector which selects said limit data when said third logic circuit result having said first voltage level is input or said numerical value data when said third logic circuit result having said first voltage level is not input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62); and

a first combiner which combines a code data (sign of the input PCM code) of said pulse code modulation data and said data selected by said second selector and which outputs a combined data (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, column 26, lines 17-19).

In regard to claim 6, Murata et al. disclose said second output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the

output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second combiner which combines a code data of said pulse code modulation data and said limit data and which outputs a combined limit data (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, column 26, lines 17-19); and

a third selector which selects said combined limit data when said third logic circuit result having said first voltage level is input or said pulse code modulation data when said third logic circuit result not having said first voltage level is input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62).

In regard to claim 7, Murata et al. discloses an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (ADPCM decoder 15, column 2, lines 31-34);

an error detector which detects whether an error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25);

a first threshold value setting portion which calculates a limit data based on said pulse code modulation data and which outputs said limit data (Fig. 28, maximum value detector 12 sets the clip value signal 114, column 26, line 66 to column 27, line 6); and

a limiter which outputs either said pulse code modulation data or a limit data in accordance with said detection result (clip processor 11, column 27, lines 12-19).

In regard to claim 16, Murata et al. disclose an apparatus for decoding encoded voice data comprising:

a demodulator which demodulates said encoded voice data and which outputs a demodulated encoded voice data (Fig. 36, conventional ADPCM reception unit 2 removes carrier wave, column 1, lines 48-50);

an adaptive differential pulse code modulation decoder which decodes said demodulated encoded voice data and which produces a pulse code modulation data (ADPCM decoder 15, column 2, lines 31-34);

an error detector which detects whether error is present in said encoded voice data and which outputs a detection result (Fig. 38, conventional error detection circuit column 2, lines 12-25);

a second threshold value setting portion which calculates a limit data based on said pulse code modulation data produced at a term and which outputs said limit data,

wherein said term is a term that a transmission error is not present in said encoded voice signal (see Fig. 29, max value detection period before T1, column 27, lines 20-29; also, Fig. 28, maximum value detector 12 sets the clip value signal 114 , column 26, line 66 to column 27, line 6); and

a limiter which outputs either said pulse code modulation data or a limit data in accordance with said detection result (clip processor 11, column 27, lines 12-19).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 8 and 17 (18) are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al., in view of Butcher et al. (U.S. Patent 4,575,863).

In regard to claim 8, Murata et al. disclose a latch portion which latches a maximal value and which outputs said maximal value based on a voltage level of a control signal (Fig. 30, when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18).

Murata et al. do not disclose determining the average value of numerical value data of said pulse code modulation data.

Butcher et al. disclose a limiter circuit that uses an average of the incoming signal to set the threshold of the limiter (column 3, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to use an average value calculation to set the threshold, instead of a maximal value, so that a large peak in the incoming PCM signal would not set the threshold of the limiter so high as to allow large bursts of noise.

In regard to claim 17, Murata et al. disclose a third output portion which stores a maximal value based on the voltage levels of a control signal and said detection results and which outputs a stored maximal value (Fig. 30, when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18).

Murata et al. do not disclose determining the average value of numerical value data of said pulse code modulation data.

Butcher et al. disclose a limiter circuit that uses an average of the incoming signal to set the threshold of the limiter (column 3, lines 1-8).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to use an average value calculation to set the threshold, instead of a maximal value, so that a large peak in the incoming PCM signal would not set the threshold of the limiter so high as to allow large bursts of noise.

In regard to claim 18, the limitation Murata et al. disclose said third output portion comprises:

a fourth logic circuit which outputs a fourth logic circuit result having said first voltage level when a voltage level of said control signal is said first voltage level and when a voltage level of said detection result is a second voltage level (Fig. 30, when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the latch to go to the limiter in the event of an error detection; since the maximum value of Murata et al. are only held in response to the error detection information 102, the circuits are equivalent) and

a second latch port in which stores said average value based on a voltage level of said fourth logic circuit result and which outputs a stored average value (when an error is detected register 12c holds the maximum amplitude value to output as the clip value, column 29, lines 12-18).

10. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al., in view of Butcher et al., and further in view of Official Notice.

Neither Murata et al. nor Butcher et al. disclose the details as to how the average calculating portion calculates an average.

Official notice is taken that it is notoriously well known in the art that an average of a signal can be found by using an average calculating portion comprising:

an accumulator which executes an addition of said numerical value data of said pulse code modulation data and a stored value, which replaces said stored value with an addition result and outputs said addition result; and

a multiple portion which executes a multiple operation of said addition result and a coefficient.

It would have been obvious to one of ordinary skill in the art at the time of invention to further modify the combination of Murata et al. and Butcher et al. so as to perform the averaging operation with an accumulator and a multiple portion, since adding the numerical data of any signal and multiplying by a coefficient (i.e. dividing by a constant) is the typical method for calculating the average of a signal.

11. Claims 10-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Murata et al., in view of Wiatrowski et al. (U.S. Patent 5,521,941).

In regard to claim 10, Murata et al. do not disclose:

a counter which counts the number of times that said pulse code modulation data is over said limit data and which outputs a count result having a first voltage level when said count result is over a predetermined value.

Wiatrowski et al. disclose system for setting a threshold value (limit) of a received signal that comprises:

a counter which counts the number of times that pulse code modulation data is over said limit data (symbol count) and which outputs a count result having a first voltage level when said count result is over a predetermined value (when a symbol is measured to be above a limit threshold, the symbol count is increased by one, until the symbol count reaches 7, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to include a counter to count the number of times pulse code modulation data is over said limit data, so that a single high value pulse code modulation data value would not set the threshold too high so as to allow bursts of noise.

In regard to claim 11, Murata et al. disclose said limit data has an upper limit data (Fig. 25, upper clip value 114) and a lower limit data (lower clip value 114); and wherein said limiter comprises:

a first comparator which compares said pulse code modulation data and said upper limit data and which outputs a first comparison result (Fig. 26, comparator 11a compares the positive amplitude of input PCM data with the clip value 114, column 26, lines 7-19);

a second comparator which compares said pulse code modulation data and said lower limit data and which outputs a second comparison result (comparator 11a compares the negative amplitude of the PCM data with the clip value 114, column 26, lines 7-19).

Murata et al. do not disclose a fourth output portion which does not output said pulse code modulation data when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 12, Murata et al. disclose a first logic circuit which outputs a first logic circuit result having a first voltage level when both a voltage level of said first comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second logic circuit which outputs a second logic circuit result having said first voltage level when both a voltage level of said second comparison result and of said detection result are said first voltage level (similarly, the negative comparison results are only activated in response to the error detection information 102, and thus the circuits are equivalent, column 25, lines 46-62); and

a first selector which selects said upper limit data when said first logic circuit result having said first voltage level is input, said lower limit data when said second logic circuit result having said first voltage level is input or said pulse code modulation data when said first and second logic circuit results each not having said first voltage level is input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62).

Murata et al. do not disclose a fourth output portion which does not output said pulse code modulation data when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 13, Murata et al. disclose a format of said limit data is the absolute value (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, therefore, the clip value must be an absolute value, column 26, lines 17-19); and wherein said limiter portion comprises:

a third comparator which compares a numerical value data of said pulse code modulation data and said limit data and which outputs a third comparison result (Fig. 26, comparator 11a, column 26, lines 7-19); and

Murata et al. do not disclose a fifth output portion which does not output said pulse code modulation data or said limit data when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 14, Murata et al. discloses said fifth output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since

the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second selector which selects said limit data when said third logic circuit result having said first voltage level is input or said numerical value data when said third logic circuit result having said first voltage level is not input (selector 11b outputs the positive and negative clip values only when a error state is detected, otherwise the unmodified PCM data is output, column 25, lines 46-62); and

a first combiner which combines a code data (sign of the input PCM code) of said pulse code modulation data and said data selected by said second selector and which outputs a combined data (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, column 26, lines 17-19).

Murata does not disclose a controller which does not output said combined data output by said first count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the combined data (PCM data with a sign bit) data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

In regard to claim 15, Murata et al. disclose said second output portion comprises:

a third logic circuit which outputs a third logic circuit result having said first voltage level when both a voltage level of said third comparison result and of said detection result are said first voltage level (see Fig. 27, output of comparator 11a is not activated until an error detected to error non-detected state is encountered, column 25, lines 46-62; the claimed 'logic circuit' is an AND gate acting as a switch to allow the output of the comparator to go to the selector in the event of an error detection; since the comparator results of Murata et al. are only output when in response to the error detection information 102, the circuits are equivalent);

a second combiner which combines a code data of said pulse code modulation data and said limit data and which outputs a combined limit data (the sign of the input PCM code must be appended to the clip value indicated by the clip value signal, column 26, lines 17-19).

Murata et al. do not disclose a third selector which does not select said combined limit data and said pulse code modulation when said count result is input having said first voltage level.

Wiatrowski et al. disclose when said count result is input, not outputting the input signal (the signal is further limited if the count exceeds the predetermined value, column 4, lines 58-66).

It would have been obvious to one of ordinary skill in the art at the time of invention to modify Murata et al. to not output the combined data (PCM data with a sign

bit) and said pulse code modulation data when said count result had said first voltage level, since this would indicate a large number of pulse code modulated data were above the limit threshold, and thus a noisy signal.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Garrigus (U.S. Patent 3,639,779) and Wisniewski (U.S. Patent 4,612,507) disclose various limiters utilizing comparators. Schorman (U.S. Patent 5,309,443) discloses an additional ADPCM decoder comprising clipper (limiter) circuits. Riedel (U.S. Patent 5,535,299) disclose an ADPCM decoder that limits the ADPCM signal prior to decoding the signal to PCM. Akira et al. (JP 09307513) and Miyata (JP 06244809) are additional references that appear from the abstract to read on at least the independent claims of the present application.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian L. Albertalli whose telephone number is (571) 272-7616. The examiner can normally be reached on Mon - Fri, 8:00 AM - 5:30 PM, every second Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on (571) 272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

BLA 10/18/05

W. R. YOUNG
PRIMARY EXAMINER